ABSTRACT OF THE DISCLOSURE

[0043] A low-power, compilable memory uses a charging pulse technique to improve access times over other low-power memory implementations. The memory includes circuitry configured to discharge a plurality of bit lines during an inactive memory access period to reduce power consumption. The memory also includes other circuitry that applies a charging pulse during an active memory access period on a select one of the plurality of bit lines in order to improve the memory access times. An automatic memory compiler adjusts a timing circuit to control the duration of the charging pulse and the enabling of a sense amplifier circuit during memory design. The memory compiler provides a programmable physical size of the memory and optimizes the access timing while ensuring reliable sensing. The compiler calculates timing for the timing circuit according to a mathematical formula that provides for highly accurate and predicable access time delays for multiple memory configurations.